CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A free-standing compliant off-chip interconnect, comprising:

a first arcuate structure;

a second arcuate structure, wherein the first arcuate structure and the second arcuate structure are disposed in substantially parallel planes; and

a middle post, wherein the first arcuate structure is connected to a lower portion of the middle post, and wherein the second arcuate structure is connected to an upper portion of the middle post.

2. The compliant off-chip interconnect of claim 1, wherein the first arcuate structure has a first mean radius and the second arcuate structure has a second mean radius, wherein the first mean radius and the second mean radius are not equivalent.

3. The compliant off-chip interconnect of claim 1 wherein the first arcuate structure has a first mean radius and the second arcuate structure has a second mean radius, wherein the first mean radius and the second mean radius are equivalent.

4. The compliant off-chip interconnect of claim 1, wherein the first arcuate structure has a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to about 100 micrometers.

5. The compliant off-chip interconnect of claim 1, wherein the second arcuate structure has a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to about 50 micrometers.

6. The compliant off-chip interconnect of claim 1, wherein the middle post has a height of about 5 to about 50 micrometers.

7. The compliant off-chip interconnect of claim 1, further comprising:

a substrate upon which the first arcuate structure and the second arcuate structure are disposed.

8. A electronic package comprising:

a substrate; and

a free-standing compliant off-chip interconnect, wherein the free-standing compliant off-chip interconnect includes a first free-standing arcuate structure that is substantially parallel to the substrate.

9. The electronic package of claim 8, wherein the free-standing compliant off-chip interconnect further includes:

a second free-standing arcuate structure that is is substantially parallel to the substrate, and wherein the first arcuate structure and the second arcuate structure are disposed in substantially parallel planes.

10. The electronic package of claim 8, wherein the first arcuate structure is connected to an assembly post.

11. The electronic package of claim 8, wherein the first arcuate structure is connected to an assembly post with a first bridge.

12. The electronic package of claim 11, wherein the first bridge includes a curved portion connecting the first arcuate structure to the assembly post.

13. The electronic package of claim 9, wherein the second arcuate structure is connected to a fabrication post with a second bridge.

14. The electronic package of claim 13, wherein the second bridge includes a curved portion connecting the second arcuate structure to the fabrication post.

15. The electronic package of claim 8, wherein the first arcuate structure has a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to about 100 micrometers.

16. The electronic package of claim 9, wherein the second arcuate structure has a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to about 100 micrometers.

17. The electronic package of claim 8, wherein the assembly post has a height of about 5 to about 50 micrometers.

18. The electronic package of claim 9, wherein the first arcuate structure has a first mean radius and the second arcuate structure has a second mean radius, wherein the first mean radius and the second mean radius are not equivalent.

19. The electronic package of claim 9, wherein the first arcuate structure has a first mean radius and the second arcuate structure has a second mean radius, wherein the first mean radius and the second mean radius are equivalent.

20. The electronic package of claim 8, wherein the substrate can be a material chosen from a semiconductor, glass, ceramic, and quartz material.

21. A method of fabricating a free-standing arcuate structure compliant off-chip interconnect, the method comprising:

depositing an arcuate structure compliant off-chip interconnect material; and

forming the free-standing arcuate structure compliant off-chip interconnect.

22. The method of claim 21, wherein depositing an arcuate structure compliant off-chip interconnect material further comprises:

forming a first arcuate structure, wherein the first arcuate structure is substantially parallel to the substrate.

23. The method of claim 22, wherein depositing an arcuate structure compliant off-chip interconnect material further comprises:

forming a second arcuate structure, wherein the first arcuate structure and the second arcuate structure are disposed in substantially parallel planes.

24. The method of claim 22, wherein depositing an arcuate structure compliant off-chip interconnect material further comprises:

forming the first arcuate structure having a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to about 100 micrometers.

25. The method of claim 23, wherein depositing an arcuate structure compliant off-chip interconnect material further comprises:

forming the second arcuate structure having a thickness of about 3 to about 30 micrometers, a width of about 5 to about 50 micrometers, and a mean radius of about 5 to about 100 micrometers.

26. The method of claim 21, wherein the substrate is chosen from semiconductor, ceramic, glass, and quartz materials.